This image is for illustration purposes only

Unbuffered Memory Module Data Sheet

MW02GN1038UA8 / MW02GN1338UA8

2 GBytes, DDR3, PC3-8500 (1066 MHz) / PC3-10600 (1333 MHz) CL8 240 Pin Unbuffered DIMM

Description:

MW02GN1038UA8 and **MW02GN1338UA8** are 2 Gigabyte Memory Modules, organized as 256Mx64 bits DDR3-SDRAM. The modules are composed by sixteen 128Mx8 DDR3-SDRAMs ICs in FBGA package forming two logical banks and one serial EEPROM for SPD (Serial Presence Detect), mounted on a JEDEC-Standard 240-pin DIMM (Dual In Line Memory Module) with golden contacts.

Features:

- Component JEDEC speed bin (CL-t_{RCD}-t_{RP}) DDR3-(8-8-8)
- 240-pin DIMM outline, unbuffered
- Dual Bank Memory Modules — Use 128Mx8 DDR3 SDRAMs
- Double Data Rate architecture; two data transfers per clock cycle
- On-Die Termination Control (ODT)
- Differential clock inputs
- Burst length (BL): 8 and 4 with Burst Chop (BC)
- Clock Cycle Time (t_{CK} avg) @ CL = 8:
  - MW02GN1338UA8: 1.50 ns
  - MW02GN1038UA8: 1.875 ns
- EEPROM Serial Presence Detection (SPD)
- Bidirectional, differential data strobe (DQS and /DQS)
- Eight internal device banks for concurrent operation
- Refresh to Active (t_{RFC}): 110 ns (min)
- Auto precharge option for each burst access
- Auto-refresh and Self-refresh modes
- Row address A_0-A_{13}
- Column address A_0-A_9
- Bank address: BA_0~BA_2
- SSTL_15 Interface: VDD = 1.5 V ± 0.075 V
- Refresh period (see note 6 below):
  - 0ºC ≤ TC ≤+85ºC : 7.8 µs
  - +85ºC < TC ≤ +95ºC: 3.9 µs

DC Characteristics
(TC=0ºC to +85ºC, VDD, VDDQ = 1.5V± 0.075V)

Parameter (NOTE: Since each bank can be in a different mode, data reflect current consumption PER BANK)	Symbol	MW02GN1038UA8	MW02GN1338UA8	Unit	Notes
		max.	max.		
Operating Current (ACT=PRE)	IDD0	680	760	mA	
Operating Current (ACT-READ-PRE)	IDD1	800	880	mA	
Precharge Power Down Standby Current	IDD2P1 IDD2P0	280 104	320 112	mA mA	Fast PD exit Slow PD exit
Precharge Quiet Standby Current	IDD2Q	440	480	mA	
Precharge Standby Current	IDD2N	440	480	mA	
Active Power-Down Current	IDD3P	280	320	mA	Always Fast exit
Active Standby Current	IDD3N	480	520	mA	
Operating Current	IDD4R IDD4W	1280 1360	1600 1680	mA mA	Burst Read operating Burst Write operating
Burst refresh Current	IDD5B	2080	2160	mA	
All Bank Interleave read current	IDD7R	2160	2480	mA	

Recommended DC Operating Conditions:
(TC = 0ºC to +85ºC) [6]

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	VDD, VDDQ	1.425	1.5	1.575	V	1,2,3
	VSS	0	0	0	V	1
	VDDSPD	3.0	3.3	3.6	V	
Input Reference Voltage	VREFCA (DC)	0.49 x VDD	0.50 x VDD	0.51 x VDD	V	1, 4, 5
Input Reference Voltage for DQ	VREFDQ (DC)	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	V	1, 4, 5

AC Characteristics:
(TC=0ºC to +85ºC, VDD, VDDQ = 1.5V± 0.075V, VSS, VSSQ = 0V)

Parameter	MW02GN1038UA8		MW02GN1338UA8		Unit (Notes)
	min.	max.	min.	max.	
tAA	15	20	12	20	ns
tWR	15	-	15	-	ns
tRCD	15	-	12	-	ns
tRRD	7.5 4	- -	6 4	- -	ns nCK
tRP	15	-	12	-	ns
tRAS	37.5	9 x tREFI	36	9 x tREFI	ns (7)
tRC	52.50	-	48.0	-	ns
tRFC	110	-	110	-	ns
tWTR	7.5 4	- -	7.5 4	- -	ns nCK
tRTP	7.5 4	- -	7.5 4	- -	ns nCK
tFAW	37.5	-	30	-	ns
tREFI	-	7.8	-	7.8	µS (6, 7)
tREFI +85ºC≤TC≤+95ºC	-	3.9	-	3.9	µS (6, 7)

Notes:
1. DDR3 SDRAM Component Specification
2. Under all conditions VDDQ must be less than or equal to VDD.
3. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together
4. The AC peak noise on VREF may not allow VREF to deviate from VREF (DC) by more than ±1% VDD (for reference: approx. ±15 mV)
5. For reference: approx. VDD/2 ±15
6. When operating in the Range +85ºC ~ +95ºC (TC = temperature of the DRAM ICs case) the following must be observed:
   a. Refresh commands must be issued at double frequency, thus t_{REF} must be lowered to 3.9µs
   b. If Self-Refresh must be used, it is mandatory to either use Manual Self-Refresh with Extended Temperature Range Capability (MR2 bits [A6, A7] = [0, 1]) or Auto Self Refresh Mode must be enabled (MR2 bits [A6, A7] = [1, 0]).
7. tREFI depends on operating case temperature (TC)

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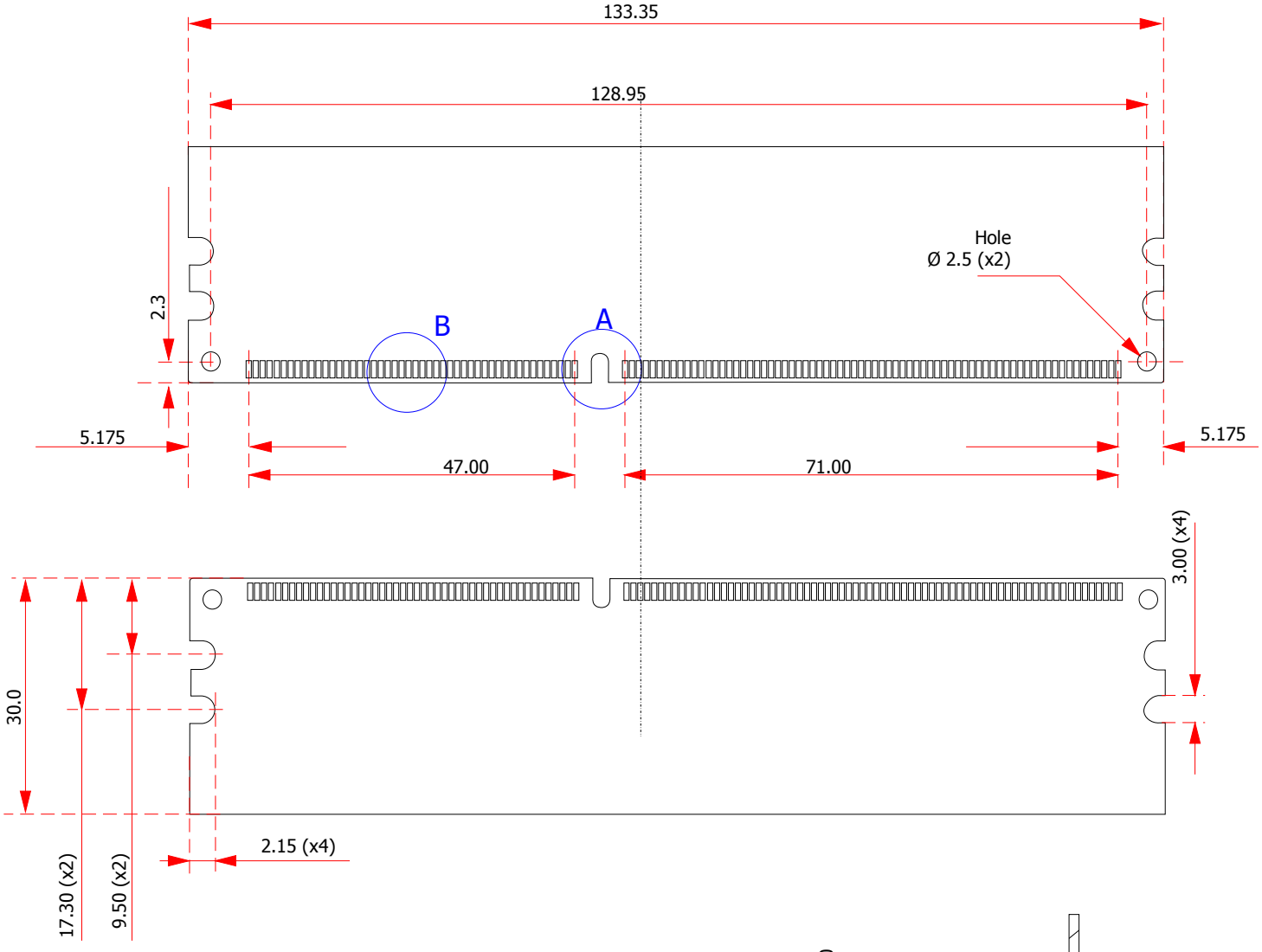
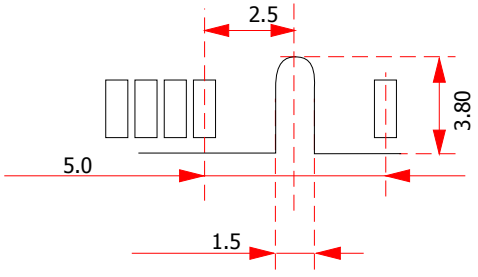
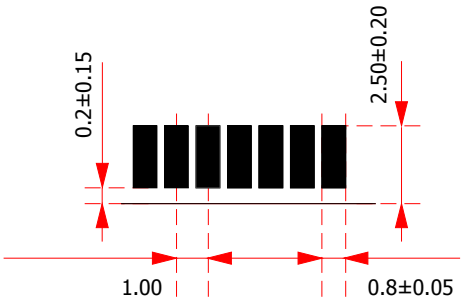
Dimensions

All dimensions are in millimeters
Tolerance is ± 0.1mm unless otherwise indicated





DETAIL A



DETAIL B