

Unbuffered Memory Module Data Sheet

MW512N5324U58

512 MBytes, DDR2, PC2-4200 (533 MHz) CL4 240 Pin DIMM

MW512N6625U58

512 MBytes, DDR2, PC2-5300 (667 MHz) CL5 240 Pin DIMM

Description:

MW512N5324U58/MW512N6625U58 are 512 Megabyte Memory Modules, organized as 64Mx64 bits DDR2-SDRAM. Each module is composed by eight 64Mx8 DDR2-SDRAMs ICs in FBGA package and one serial EEPROM for SPD (Serial Presence Detect), mounted on a JEDEC-Standard 240-pin DIMM (Dual In Line Memory Module) with golden contacts.

Features:

- 240-pin DIMM outline, unbuffered
- Double Data Rate architecture; two data transfers per clock cycle
- On-Die Termination Control
- Uses 64Mx8 DDR2-SDRAMs
- Differential clock inputs
- Programmable burst length: 4 or 8
- Clock Cycle Time (MW512N5324U58)
 - (t_{CK}) = 3.75 ns (min.) / 8 ns (max.) @ CL=4
- Clock Cycle Time (MW512N6625U58)
 - (t_{CK}) = 3.00 ns (min.) / 8 ns (max.) @ CL=5
- EEPROM Serial Presence Detection (SPD)
- Bidirectional, differential data strobe (DQS and /DQS)
- Four internal device banks for concurrent operation
- Auto Refresh to Active (t_{RFC}): 105ns (min)
- Auto precharge
- Auto-refresh and Self-refresh modes
- Row address A₀-A₁₃
- Column address A₀-A₉
- SSTL_18 Interface
- VDD = VDDQ = 1.8 V ± 0.1 V

Specification:

Symbol	AC Characteristic	Min.	Max.	Unit	
t_{CK}	CLK Cycle Time	MW512N5324U58 CL=4	3750	8000	ps
		MW512N6625U58 CL=5	3000		
t_{RC}	Row Cycle Time (Operation)	60	-	ns	
t_{RAS}	Row Active Time	45	70,000	ns	
t_{RFC}	Auto Refresh to Active / Auto Refresh Command Time	105	-	ns	

Ratings:

	Rating	Unit	Condition
Power Dissipation, Operating (Row Activating, Precharge) @VDD, VDDQ = 1.8V	1.584	W	Ta=25°C
	1.656		
Operating temperature ¹	0 ~ 85	°C	
Storage temperature	-55 ~ 100	°C	

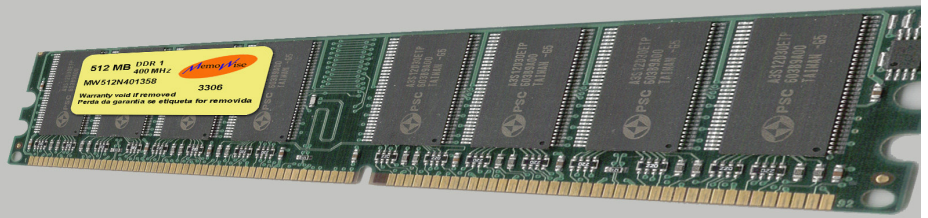
Note:

1. It refers to the operating case temperature of DRAM ICs

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Dimensions

All dimensions are in millimeters (Inches); tolerance is ± 0.127 (0.005") unless otherwise indicated

